DC/1(a)/ Jul/2022

# **EXPERIMENT NO.1 (a)**

**TITLE**: **Study of the PN Sequence generation.**

**OBJECTIVE:** a)Design and implementation of 15 bit PN (pseudo noise) sequence using shift register.

b) Verify the properties of the sequence

c) Observe the spectrum of PN sequence using spectrum analyzer.

d) Measure the band width of the sequence.

**EQUIPMENT/COMPONENT REQUIRED:**

S. No. ITEMS Qty.

1. Power Supply +5v 01

2. CRO 01

3. Function generator 01

S.No. ITEMS QTY

4. IC 74164 shift register 01

5. IC 7486 01

6. Bread board 01

7. Connecting wires

**THEORY:** A Pseudo-Noise (PN) sequence is a periodic binary sequence with a noise-like waveform that is usually generated by means of a Linear Feedback Shift Registers (LFSR). It has applications in scrambling, cryptography, and spread-spectrum communications. It is also commonly referred to as the Pseudo-Random Binary Sequence (PRBS). These are very widely used in communication standards these days. The qualifier "pseudo" implies that the sequence is not truly random. Actually, it is periodic with a (possibly large) period, and exhibits some characteristics of a random white sequence within that period. A general block diagram of a LFSR is shown in the following figure:

C.P.

DA QA

CP

DC QC

CP

DD QD

Combinational logic ckt.

CP

DB QB

C.P.

Clock Pulse Generator

74164

PN Sequence

7486

A feedback shift register consists of an ordinary shift register made up of m flip-flops (Two-stage memory stages) and a logic circuit that are interconnected to form a multi-loop feedback circuit. The flip –flops in the shift register are regulated by a single timing clock. At each pulse of the clock, the state of each flip-flop is shifted to the next one down the line. The output contains a Boolean function of the states of the flip-flops. The result is then fed back as the input to the first flip-flop, thereby preventing the shift register from emptying. The PN sequence so generated is determined by the length m of the shift register, its initial state and the feed-back logic.

A feedback shift register is said to be linear when the feed-back logic consists entirely of modulo 2 adders. In such a case, the all-zero state is not permitted. We say so because if the state of the shift register is all zero at any time, it remains so for all time. We need to ensure that this never happens (we start with a non-zero value). The period of a PN sequence produced by a linear feed-back shift register with m flip-flops cannot exceed 2m -1. When the period is exactly 2m -1, the PN sequence is called maximal length PN sequence or simply m - sequence.

Properties of PN Sequence: There are several properties of a PN sequence. But we are mentioning only those we are verifying in this experiment.

* Balance Property: Number of 1’s is always one more than number of 0’s.
* Run Property: A run is string of consecutive 1’s or a string of consecutive 0’s. In any m-sequence, one-half of the runs have length 1, one quarter has length 2, and one-eighth has length 3, and so on. If length of the sequence is N, then total no. of runs = (N + 1)/2.
* Auto Correlation Property: The auto Correlation function of a maximal length sequence is periodic and binary valued.

N. B: By definition, the auto Correlation function of a periodic signal c (t) of period Tb is,

Rc (τ) = τ) dt

**EXPERIMENTAL PROCEDURE:**

**Follow the sequence given below:--**

1. Assemble the circuit on breadboard as shown in fig. Connect the power supply +5volt.
2. Set the clock frequency of function generator at 20 KHz.
3. Display the o/p sequence pattern on CRO from pin no.6 (QD) of 74164. Draw the clock pulse and o/p sequence pattern in graph paper. Also observe the spectrum of the o/p sequence. Measure the bandwidth.
4. Change the combinational logic function and repeat the procedure for **(QB or QC)** for different sequences of PN sequence. 

**Circuit Diagram:**



14

7

Pin Configuration of 74164

GND

**OBSERVATIONS:**

1. Draw the clock pulse signal and 15-bit PN sequence pattern in graph paper.

2. Show the Spectrum of PN Sequence & measure the Band Width of the Spectrum using spectrum analyzer.

**NETAJI SUBHASH ENGINEERING COLLEGE**

Department of Electronics & Communication Engg.

**Digital Communication Lab**

ECE 3rd YEAR 6th SEM

**WORK SHEET**

# **EXPERIMENT NO.1 (a)**

**TITLE**: **Study of the PN Sequence generation.**

**OBJECT:** a)Design and implementation of 15 bit PN (pseudo noise) sequence using shift register.

b) Study the properties of the sequence

c) Observe the spectrum of PN sequence using spectrum analyzer.

d) Measure the band width of the sequcnce

**EQUIPMENT/COMPONENT REQUIRED:**

S. No. ITEM Qnty. Specification

1. Power Supply +5v 01

2. CRO 01

3. IC 74164 01

4. IC 7486 01

6. Bread board 01

7. Connecting wires

**Result:**

1. Feedback connection **Qa Xor Qd:** Write & draw 15-bit sequence:

Justify the above sequence with the properties of PN sequence:

2. Feedback connection **Qb Xor Qd** Write down 15-bit sequence:

Justify the above sequence with the properties of PN sequence:

3. Feedback connection **Qc Xor Qd** Write down 15-bit sequence**:**

Justify the above sequence with the properties of PN sequence:

4. Draw the sample spectrum show the bandwidth

**FURNISH YOUR LAB REPORT WITH:**

**1. Name of exp. 2. Objective 3. Brief theory. 4 .Equipment & Component required with specification. 5. Circuit / block**

**diagram 6. Work sheet 8. Graph /Wave form/Spectrum 9. Discussion**